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EXAMINER	
MILORD, MARCEAU	
ART UNIT	**PAPER NUMBER**
2682	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/692,508	WU ET AL.	
	Examiner	Art Unit	
	Marceau Milord	2682	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-103* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-103* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-103 are rejected under 35 U.S.C. 103(a) as being unpatentable over Narumi et al (US Patent No 6118811) in view of Ando (US Patent No 5949285).

Regarding claims 1, 11, 15, Narumi et al discloses a calibration circuit (figs.1-3, 5), comprising: a first component (150 of fig. 1); a digitally tunable second component (50 of fig. 1; col. 1, line 65- col. 2, line 10; col. 5, lines 17-59); and a logic control (130 and 60 of fig. 1) block to digitally tune the second component as a function of the first and second parameters (col. 3, line 46- col. 4, line 21; col. 6, lines 9-67).

However, Narumi et al does not specifically disclose the feature of a current source coupled to the first component to generate a first parameter of the first component, and coupled to the second component to generate a second parameter of the second component.

On the other hand, Ando, from the same field of endeavor, discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55) Furthermore, a seventh

transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Claims 2-4 contain similar limitations addressed in claim 1, and therefore are rejected under a similar rationale.

Regarding claim 5, Narumi et al as modified discloses a calibration circuit (figs.1-3, 5) wherein the first parameter comprises a first voltage and the second parameter comprises a second voltage (col. 5, lines 31-43; col. 6, lines 9-32; col. 6, lines 55-67).

Regarding claim 6, Narumi et al as modified discloses a calibration circuit (figs.1-3, 5) wherein the logic control block comprises a comparator to compare the first and second voltages, and control logic to digitally tune the second component as a function of the voltage comparison (col. 6, lines 22-61).

Regarding claims 7-10, 12-14, 16, Narumi et al as applied to claim 1 above differs from claims 7-10, 12-14, 16-17 in that Narumi fails to disclose the features of the first component comprises a resistor, the second component comprises a second resistor; and the second resistor comprises a tunable resistor array.

However, Ando discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col.

5, line. 3- col. 6, line 55). Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Claim 17 contains similar limitations addressed in claim 1, and therefore is rejected under a similar rationale.

Regarding claims 18-19, 30, 35, Narumi et al discloses a calibration circuit (figs.1-3, 5), comprising: a first component (150 of fig. 1); a digitally tunable second component (50 of fig. 1); and a second parameter of the second component (col. 1, line 65- col. 2, line 10; col. 5, lines 17-59); and tuning means (130 and 60 of fig. 1) for digitally tuning the second component as a function of the first and second parameters (col. 3, line 46- col. 4, line 21; col. 6, lines 9-67).

However, Narumi et al does not specifically disclose the feature of a generating means wherein the generating means comprises a current source for generating a first parameter of the first component.

On the other hand, Ando, from the same field of endeavor, discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55) Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a

second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Claims 20-23 contain similar limitations addressed in claim 18, and therefore are rejected under a similar rationale.

Regarding claim 24, Narumi et al as modified discloses a calibration circuit (figs.1-3, 5), wherein the tuning means comprises a comparator to compare the first and second voltages, and control logic to digitally tune the second component as a function of the voltage comparison (col. 6, lines 22-61).

Regarding claims 25-29, 31-34, 36-37, Narumi et al as applied to claim 18 above differs from claims 25-29, 31-34, 36-37 in that Narumi fails to disclose the features of the first component comprises a resistor, the second component comprises a second resistor; and the second resistor comprises a tunable resistor array.

However, Ando discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55). Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply

the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Regarding claim 38, Narumi et al discloses a calibration circuit (figs.1-3, 5), comprising: a first component (150 of fig. 1); a digitally tunable second component (50 of fig. 1); coupled to the current through a second node (col. 1, line 65- col. 2, line 10; col. 5, lines 17-59); a comparator having an input coupled to the first and second nodes, and an output; and control logic (130 and 60 of fig. 1) coupled between the output of the comparator and the second component (col. 3, line 46- col. 4, line 21; col. 6, lines 9-67).

However, Narumi et al does not specifically disclose the feature of a current source; a first component coupled to the current source through a first node.

On the other hand, Ando, from the same field of endeavor, discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55) Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Claims 39-40 contain similar limitations addressed in claim 38, and therefore are rejected under a similar rationale

Regarding claims 41-49, Narumi et al as applied to claim 38 above differs from claims 41-49 in that Narumi fails to disclose the features of the first component comprises a resistor, the second component comprises a second resistor; and the second resistor comprises a tunable resistor array.

However, Ando discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55). Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Regarding claims 50, 60, 68, Narumi et al discloses a transceiver (fig. 1), comprising: a calibration circuit (figs. 2-4) comprising a first component (150 of fig. 1), a digitally tunable second component (50 of fig. 1; col. 1, line 65- col. 2, line 10; col. 5, lines 17-59), and a logic control block (130 and 60 of fig. 1) having a control output to digitally tune the second component as a function of the first and second parameters; and a digitally tunable transceiver component tuned by the control output of the logic control block (col. 3, line 46- col. 4, line 21; col. 6, lines 9-67).

However, Narumi et al does not specifically disclose the feature of a current source coupled to the second component to generate a second parameter of the second component coupled to the first component to generate a first parameter of the first component.

On the other hand, Ando, from the same field of endeavor, discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55) Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Claims 51-53 contain similar limitations addressed in claim 50, and therefore are rejected under a similar rationale.

Regarding claim 54, Narumi et al as modified discloses a transceiver (fig. 1), comprising: a calibration circuit (figs. 2-4) wherein the first parameter comprises a first voltage and the second parameter comprises a second voltage (col. 3, lines 24-45; col. 5, lines 30-55).

Regarding claim 55, Narumi et al as modified discloses a transceiver (fig. 1), comprising: a calibration circuit (figs. 2-4) wherein the logic control block comprises a comparator to compare the first and second voltages, and control logic comprising the control output to digitally tune the second component as a function of the voltage comparison (col. 6, lines 22-61).

Regarding claims 56-59, 61-67, 69-74, Narumi et al as applied to claim 50 above differs from claims 56-59, 61-67, 68-74 in that Narumi fails to disclose the features of the first component comprises a resistor, the second component comprises a second resistor; and the second resistor comprises a tunable resistor array.

However, Ando discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55). Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Regarding claims 75, 77-78, 85, Narumi et al discloses a transceiver (fig. 1), comprising: a calibration circuit (figs. 2-4) comprising a first component (150 of fig. 1), a digitally tunable second component (50 of fig. 1), a current coupled to the first component to generate a first parameter of the first component and coupled to the second component to generate a second parameter of the second component (col. 1, line 65- col. 2, line 10; col. 5, lines 17-59), and a logic control block (130 and 60 of fig. 1) having a control output to digitally tune the second component as a function of the first and second parameters(col. 3, line 46- col. 4, line 21; col. 6, lines 9-67).

However, Narumi et al does not specifically disclose the feature of a current source coupled to the first component to generate a first parameter of the first component; and bandgag calibration circuit to generate a bandgag current substantially independent of temperature, the bandgag calibration circuit being responsive to the control output from the logic control block.

On the other hand, Ando, from the same field of endeavor, discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55) Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Regarding claim 76, Narumi et al as modified discloses a transceiver (fig. 1), comprising: a calibration circuit (figs. 2-4) wherein the current source provides a first current to the first component and a second current to the second component (col. 3, lines 28-42; col. 5, lines 31-47).

Regarding claim 79, Narumi et al as modified discloses a transceiver (fig. 1), comprising: a calibration circuit (figs. 2-4) wherein the first parameter comprises a first voltage and the second parameter comprises a second voltage (col. 5, lines 31-43; col. 6, lines 9-32; col. 6, lines 55-67).

Regarding claim 80, Narumi et al as modified discloses a transceiver (fig. 1), comprising: a calibration circuit (figs. 2-4) wherein the logic control block comprises a comparator to compare the first and second voltages, and control logic comprising the control output to digitally tune the second component as a function of the voltage comparison (col. 6, lines 22-61).

Regarding claims 81-84, 86-87, Narumi et al as applied to claim 75 above differs from claims 81-84, 86-87 in that Narumi fails to disclose the features of the first component comprises a resistor, the second component comprises a second resistor; and the second resistor comprises a tunable resistor array.

However, Ando discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55). Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Regarding claims 88, 94-99, Narumi et al discloses a method of calibration (figs.1-3, 5), comprising: providing a current to a second component to generate a second parameter (col. 1, line 65- col. 2, line 10; col. 5, lines 17-59); and digitally tuning the second component as a function of the first and second parameters (col. 3, line 46- col. 4, line 21; col. 6, lines 9-67).

However, Narumi et al does not specifically disclose the step of providing a first current to a first component to generate a first parameter.

On the other hand, Ando, from the same field of endeavor, discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55) Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Regarding claim 89, Narumi et al as modified discloses a method of calibration (figs.1-3, 5), wherein the first current is substantially equal to the second current (col. 4, lines 1-32).

Regarding claim 90, Narumi et al as modified discloses a method of calibration, (figs.1-3, 5), comprising generating a reference current, and mirroring the first and second currents to the reference current (col. 3, lines 24-45; col. 5, lines 30-55).

Regarding claims 91-93, 100-103, Narumi et al as applied to claim 88 above differs from claims 91-93, 100-103 in that Narumi fails to disclose the features of the second component comprises a plurality of resistors coupled in series, and the digital tuning of the second component comprises selectively bypassing at least one of the resistors; the second component comprises a plurality of capacitors coupled in a parallel array, and the digital tuning of the

second component comprises selectively switching at least one of the capacitors in or out of the array.

However, Ando discloses a gain variable amplifier where a first differential amplifier is formed by first and second transistors having a common emitter connected to a first constant current source, a second differential amplifier is formed by third and fourth transistors having a common emitter connected to a collector of the second transistor, and a third differential amplifier is formed by fifth and sixth transistors having a common emitter (col. 2,lines 1-10; col. 5, line. 3- col. 6, line 55). Furthermore, a seventh transistor is connected between the common emitter of the fifth and sixth transistors and a second constant current source. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Ando to the system of Narumi in order to control the gain by the gain control voltage.

Response to Arguments

2. Applicant's arguments with respect to claims 1-103 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 703-306-3023. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Vivian C. Chin can be reached on 703-308-6739. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARCEAU MILORD

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Examiner
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